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ROYAL SIGNALS & RADAR ESTABLISHMENT

ENHANCED PERFORMANCE IR FOCAL PLANE ARRAYS USING ADAPTIVE SUBTRACTION

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TITLE: Enhanced Performance IR Focal Plane Arrays Using Adaptive Subtraction

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SUMMARY

This memorandum describes a compact, adaptive circuit, realisable at the pixel level of Infrared focal plane detector arrays. The technique removes unwanted currents from the array, permitting more signal current to be integrated at the pixel. This can be used to improve performance, improve uniformity of signals from the array and simplify associated electronics. The choice of advantage conferred by this scheme depends on the system in which it is employed.

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ENHANCED PEFORMANCE IR FOCAL PLANE ARRAYS USING ADAPTIVE SUBTRACTION

R A Ballingall and I D Blenkinsop

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1. INTRODUCTION

Photovoltaic focal plane arrays operating in the medium and long infrared wavebands can suffer performance limitations due to unwanted pedestal curents. In terrestrial applications this pedestal current is typically several times greater than the required dynamic range of the focal plane array (FPA). This problem is most severe if, in an attempt to achieve fully staring performance, FPA's use current integration at the pixel. Many arrays presently available use this technique. However, in the long waveband, this approach fails due to the inability to store the large currents coming from the detectors. In this memorandum we describe a scheme which overcomes this limitation and allows considerable improvement in FPA performance.

Unwanted detector currents may arise from a variety of sources, which depend on the array configuration and the application in which it is used. The most basic source is that of infrared emission from the ambient temperature background (ref 1). In some applications, notably in high speed missiles and aircraft, a further large contribution may be made by optics and windows heated above ambient temperature by aerodynamic effects. (Note that this heating may vary with time of flight or velocity).

A leakage current, not associated with infrared radiation, may also be present. This is present when the detector is operated in reverse bias, which may be done for several reasons. The main reasons are, firstly to increase diode impedance and secondly to accommodate the spread in offset voltges inherent in Silicon readout circuits.

Although these problems are present in high performance detectors, they become increasingly severe as operating temperature is increased, for example in NDI photon detectors (ref 2).

Regardless of the source; the unwanted current may be removed by the scheme described here. Hence this offers considerable performance improvements in a wide range of applications. An additional advantage of this scheme is that it can reduce both the speed and dynamic range of the electrical signals at the output of the array. This in turn reduces the cost, size and power of the system containing the FPA.

2. THE PROBLEM

The problem of unwanted pedestal currents is common to many FPA configurations and several solutions have been put forward (refs 3 and 4). These have met with limited success because, in general, they attempt to subtract the same amount of charge from each element of the array. This ignores the non-uniformity between pixels which dominates the dynamic range of high performance arrays (ref 5).

The problems are illustrated in figure 1, which shows the I-V characteristics and load line for a single diode. A signal current, due to variations in the scene, ΔI_p, is superimposed on a much larger unwanted photocurrent I_p. If the diode is operated at zero bias, only this current I_p needs to be subtracted. Even if an attempt is made to operate at zero bias, variations in the load lines from pixel to pixel force some detectors into reverse bias. However in many cases the diodes are deliberately operated in reverse bias in order to increase their slope resistance above R_o. This results in improved injection efficiency and hence in greater signal to noise ratio. Reverse bias operation results in the addition of a leakage current, I_l, to the photocurrent. In this case it is desirable to subtract the total current ($I_t = I_l + I_p$), leaving a nett signal current, ΔI_t. The current I_l may be due to a variety of processes. However, regardless of its source, it increases non-uniformity of currents between pixels. The overall result of reverse bias operation is an increase in both the unwanted currents and the non-uniformity between pixels.

3. THE IDEAL SOLUTION

The solution to the problem outlined above is the subtraction of the unwanted current, I_t which has a different value at each pixel. Ideally this should compensate for differences between detectors, optics and the inputs of the read-out circuits. To utilise the advantage of integration at the pixel, this function must be achieved within each pixel. This implies that the circuity must be of small volume and low power.

Our proposed solution, which is the subject of a UK patent (ref 6) consists essentially of a programmable current source coupled to a current summing node which subtracts the current I_t from the incoming current from the detector ($I_t + \Delta I_t$). To achieve the stated aims, the current sources must be programmed with currents appropriate to each detector channel.

The optimum way to do this is to make the current sources self-programming to values which are exactly equal to the currents coming from the input channels viewing a uniform scene. A possible implementation of this is shown in figure 2.

Figure 2 shows a channel consisting of a photovoltaic detector connected to a current amplifier which can, in practice, consist of a direct injection (DIG) circuit. Output current from this is integrated on a capacitor, C_s, which can be reset to a fixed voltage, V_{RS}, via transistor T_1. The voltage on C_s is buffered by a source follower T_2 before connection to an output multiplexer. These elements of the circuit are conventional. Usually the value of C_s is made as large as possible within the available area (typically 50 x 50 μm). The novel part of the circuit is shown within the dotted box in figure 2. Transistor T_3 acts as a constant current source in which the current is set by the voltage upon capacitor C_c. The voltage on C_c is programmed during a calibration phase. To perform this calibration, the detector array is exposed to a uniform scene. Transistor T_7 is briefly

switched on to reset the voltage on C_c. Transistors T_4 and T_6 are then turned on. This results in the voltage on C_s falling which, via T_4 and T_5, sets the voltage on C_c. When the voltage on C_s is such that the current in T_3 is equal to I_t, the voltages on C_s and C_c settle to equilibrium vales. When this condition is achieved, T_4 is turned off leaving a fixed, programmed voltage on C_c which can maintain the fixed current I_t flowing in T_3 and T_6. Subsequent operation consists of periods of integration followed by readout and resetting of the voltage on C_s. Transistor T_6 may be used to turn off the subtracted current during the reset period. To maintain constant current in T_3 a bias voltage must be applied between its gate and drain. Transistor T_5 acts as a fixed voltage source to ensure that this condition is always met.

The constancy of subtracted current, I_t, is determined by leakage of capacitor C_c and the surrounding transistors. This mechanism will determine the interval between calibrations. These leakage currents are highly sensitive to temperature and, in cryogenic operation, the calibration interval can be greater than many minutes. Although capacitor C_c and the associated transistors consume space within the pixel, the amount of charge that needs to be stored on C_s is now substantially reduced. This allows the integration time to be increased, even with the reduced area available for C_s. In practice the accuracy of the programming voltage left on C_c is determined by the feedthrough charge injected through T_4 and the value of the capacitor. This results in an error term which is different for each pixel, but reproducible between calibration cycles. The magnitudes of these errors will depend upon the technology used and are likely to set a practical limit to the value of unwanted current which may be subtracted.

4. TECHNOLOGY

The chief technological problem in implementing this scheme is one of area. In a well laid out circuit, most of the available Si area should be used for the two capacitors, of which C_s should be the larger. Note that the dynamic range at the output of the circuit (ΔI_t in figure 1) still depends upon the value of charge which may be stored on C_s. For this reason, any increase of capacitance brought about by the use of high dielectric constant materials or by increase in area will furhter improve the signal to noise ratio.

In cases where adequate dynamic range cannot be achieved using the value of C_s fabricated in the area of a single pixel, an alternative approach is to use a sparse array. For example a 50 x 50 μm detector may be fitted into a 100 x 100 μm area of Si and microscanned to produce an image. This results in a sensitivity which can only be half that of a fully staring array. However, the greatly increased area available for storage capacitance may make it much easier to attain this performance in practice.

To successfully demonstrate the principle described here, the technology employed must use components with low leakage and low feed through charge. The basic circuit action has been demonstrated in breadboard form using commercial discrete components. However it is impractical to use this approach with realistic capacitor values ($\leq$ 1pF).

In order to progress the idea further, the circuits are at present being fabricated using standard CMOS technology.

5. CONCLUSION

The scheme described here offers an improvement in performance which may be exploited in one of three ways or in a combination of all.

i) Improved sensitivity in terms of smaller NETD.

ii) Reduced speed for a given sensitivity, ie slower clock generators, A/D converters and processing electronics, which will be lower in power and cheaper to implement.

iii) Reduced dynamic range for a given sensitivity, ie fewer bits in the A/D convertors and associated electronics.

The way in which the improvement can be exploited depends on the system configuration and on the waveband in which the detector operates. In the 3-5 μm waveband, where photocurrent is typically of the order of 1nA, the main advantage of adaptive subtraction will be in items (ii) and (iii). In the 8-14 μm band detector configurations, which have been hitherto impractical, can now be implemented. This should result in the realisation of arrays giving better than line equivalent performance; possibly approaching fully staring under some circumstances (see figure 3).

Under some circumstances the current from a detector may be greater than that expected from a BLIP detector viewing a typical, terrestrial scene. An obvious example of this is a detector operated at elevated temperature, where the leakage current has increased. Under these conditions, very large capacitors would be required on the focal plane to accommodate this increased current. The scheme described allows larger arrays to be fabricated using NDI detectors (ref 2).

A similar problem exists in high speed missile applications where aerodynamic window heating adds to the background pedestal signal. In this case the advantage chosen would probably be in terms of increased sensitivity, resulting in longer range.

In conclusion, we have described a compact, adaptive circuit, realisable at the pixel level. This can improve performance, simplify the associated electronics and improve the uniformity of signals from an array. These improvements have not yet been fully quantified, but experiments to measure them are in progress.

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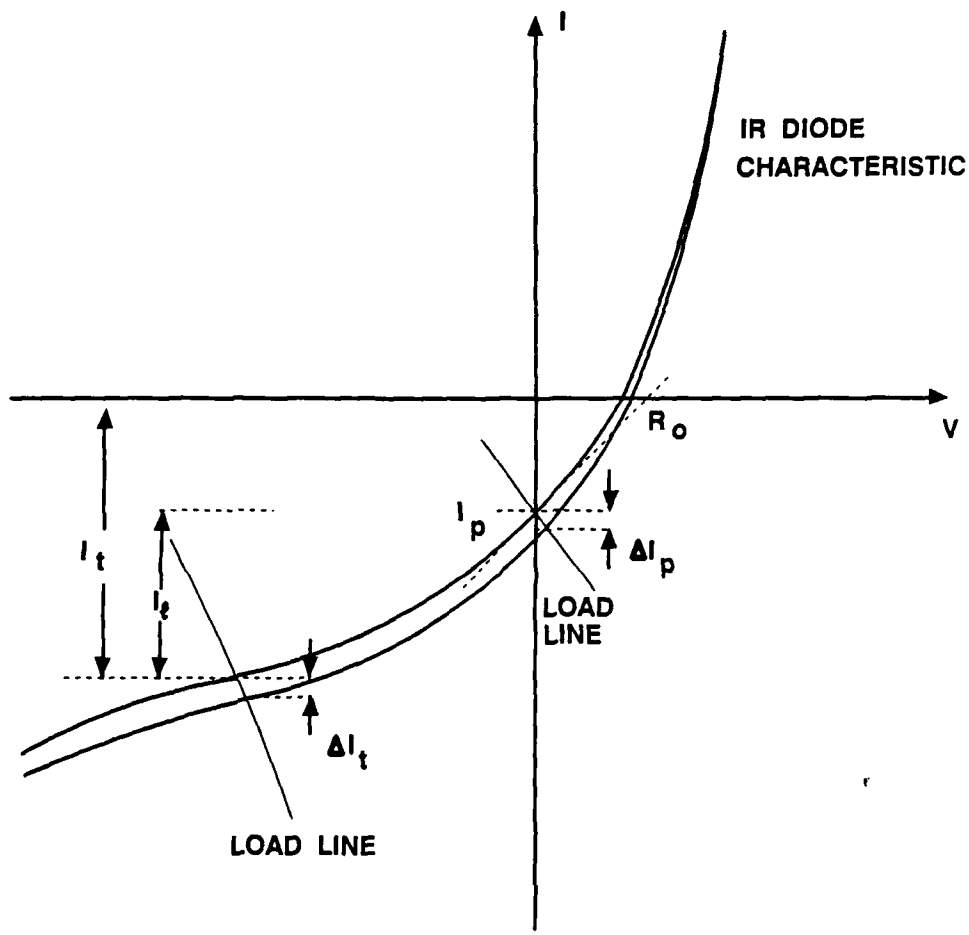

FIGURE 1. OPERATING POINTS FOR ONE PIXEL IN AN ARRAY

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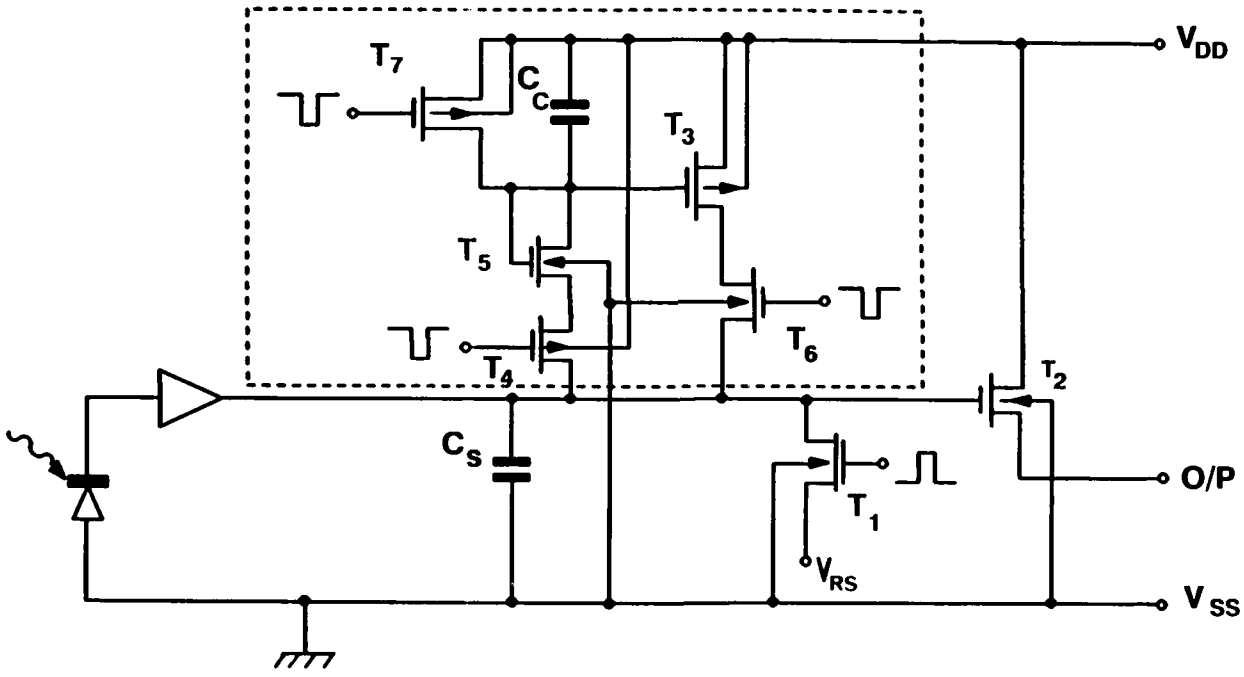
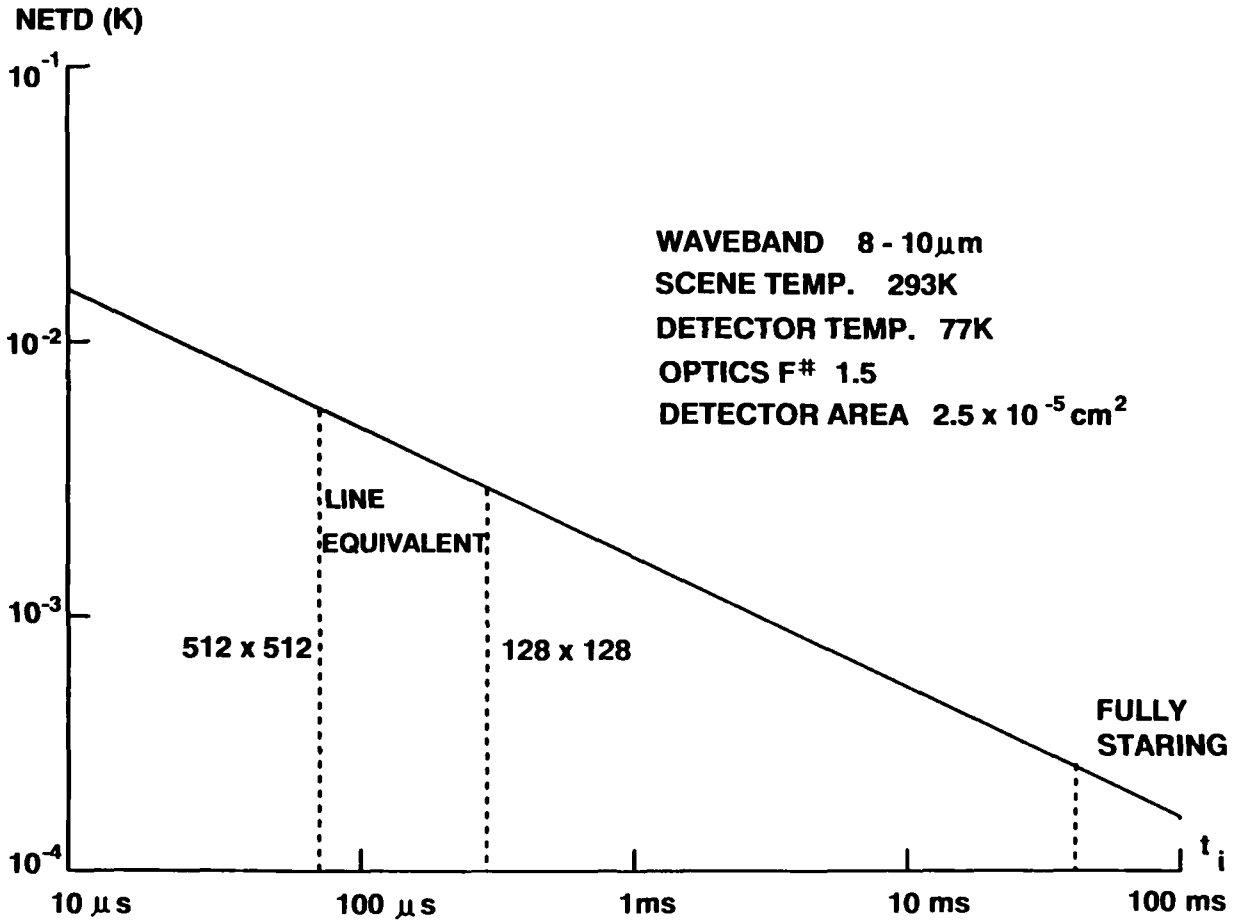


Figure 2. ADAPTIVE SUBTRACTION CIRCUIT

Figure 3. THEORETICAL NOISE EQUIVALENT TEMPERATURE DIFFERENCE vs t_i



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Abstract

This memorandum describes a compact, adaptive circuit, realisable at the pixel level of Infrared focal plane detector arrays. The technique removes unwanted currents from the array, permitting more signal current to be integrated at the pixel. This can be used to improve performance, improve uniformity of signals from the array and simplify associated electronics. The choice of advantage conferred by this scheme depends on the system in which it is employed.